ANALOG DEVICES

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APPLICATION NOTE

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# A Tamper-Resistant Watt-Hour Energy Meter Based on the AD7751 and Two Current Sensors

by Anthony Collins and William Koon

## INTRODUCTION

This application note describes a low-cost, high-accuracy watt-hour meter based on the AD7751. The meter described is intended for use in single-phase, two-wire distribution systems. However, the design can easily be adapted to suit specific regional requirements, e.g., in the United States power is usually distributed to residential customers as single-phase, three-wire.

The AD7751 is a low-cost, single-chip solution for electrical energy measurement. The most distinctive feature of the AD7751 is that it continuously monitors the phase and neutral (return) currents. A FAULT condition occurs if the two currents differ by more than 12.5%. Power calculation will be based on the larger of the two currents. The meter calculates power correctly even if one of the two wires does not carry any current. AD7751 provides an effective way to combat any attempt to return the current through earth, a very simple yet effective way of meter tampering. The AD7751 is comprised of two ADCs, reference circuit, and all the signal processing necessary for the calculation of real (active) power. The AD7751 also includes direct drive capability for electromechanical counters (i.e., the energy register) and has a high-frequency pulse output for calibration and communications purposes.

This application note should be used in conjunction with the AD7751 data sheet. The data sheet provides detailed information on the functionality of the AD7751 and will be referenced several times in this application note.

## DESIGN GOALS

The International Standard IEC1036 (1996-09)—*Alternating current watt-hour meters for active energy (Classes 1 and 2)*, was used as the primary specification for this design. For readers more familiar with the ANSI C12.16 specification, see the section at the end of this application which compares the IEC1036 and ANSI C12.16 standards. This section explains the key IEC1036 specifications in terms of their ANSI equivalents.

The design greatly exceeds this basic specification for many of the accuracy requirements, e.g., accuracy at unity power factor and at low (PF = ±0.5) power factor. In addition, the dynamic range performance of the meter has been extended to 500. The IEC1036 standard specifies accuracy over a range of 5% Ib to $I_{MAX}$—see Table I. Typical values for $I_{MAX}$ are 400% to 600% of Ib. Table I outlines the accuracy requirements for a static watt-hour meter. The current range (dynamic range) for accuracy is specified in terms of Ib (basic current).

**Table I. Accuracy Requirements**

| Current Value[1] | PF[2] | Percentage Error Limits[3] Class 1 | Class 2 |
|---|---|---|---|
| 0.05 Ib ≤ I < 0.1 Ib | 1 | ±1.5% | ±2.5% |
| 0.1 Ib ≤ I ≤ $I_{MAX}$ | 1 | ±1.0% | ±2.0% |
| 0.1 Ib ≤ I ≤ 0.2 Ib | 0.5 Lag | ±1.5% | ±2.5% |
| | 0.8 Lead | ±1.5% | — |
| 0.2 Ib ≤ I ≤ $I_{MAX}$ | 0.5 Lag | ±1.0% | ±2.0% |
| | 0.8 Lead | ±1.0% | — |

NOTES

[1]The current ranges for specified accuracy shown in Table I are expressed in terms of the basic current (Ib). The basic current is defined in IEC1036 (1996-09) Section 3.5.1.1 as the value of current in accordance with which the relevant performance of a direct connection meter is fixed. $I_{MAX}$ is the maximum current at which accuracy is maintained.

[2]Power Factor (PF) in Table I relates the phase relationship between the fundamental (45 Hz to 65 Hz) voltage and current waveforms. PF in this case can be simply defined as PF = cos(ϕ), where ϕ is the phase angle between pure sinusoidal current and voltage.

[3]Class index is defined in IEC1036 (1996-09) Section 3.5.5 as the limits of the permissible percentage error. The percentage error is defined as:

$$Percentage\ Error = \frac{energy\ registered\ by\ meter - true\ energy}{true\ energy} \times 100\%$$

The schematic in Figure 1 shows the implementation of a simple, low-cost watt-hour meter using the AD7751. Two current transformers (CTs) are used to provide the current-to-voltage conversion needed by the AD7751, and a simple divider network attenuates the line voltage. The energy register (kWhrs) is a simple electromechanical counter that uses a two-phase stepper motor. The AD7751 provides direct drive capability for this type of counter. The AD7751 also provides a high-frequency output at the CF pin for the meter constant (e.g., 3200 imp/kWhr). Thus a high-frequency output is available at the LED and opto-isolator output. This high-frequency output is used to speed up the calibration process and provides a means of quickly verifying meter functionality

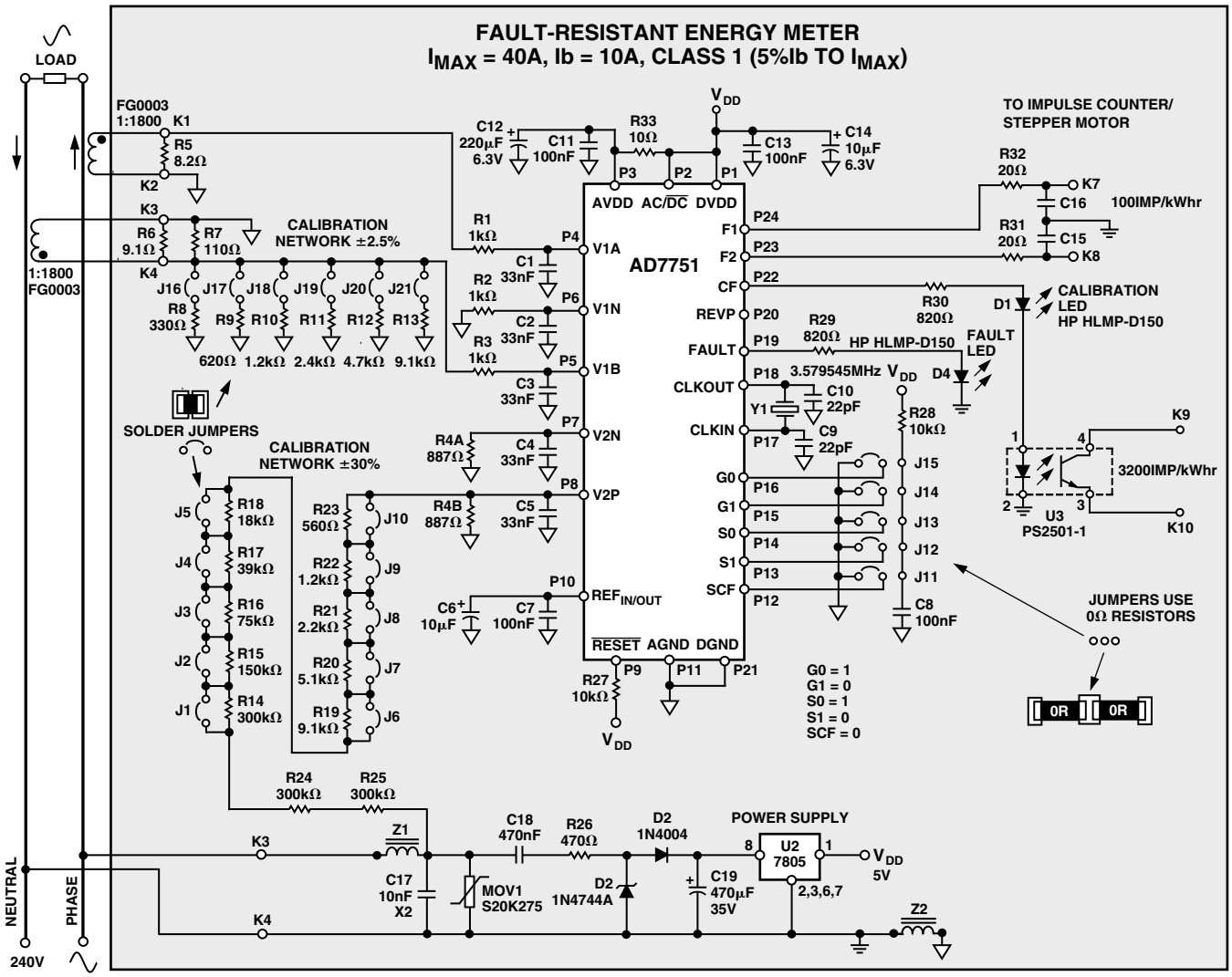



*Figure 1. Simple Single-Phase Watt-Hour Meter Based on the AD7751*

and accuracy in a production environment. The meter is calibrated in a two-step process:

Step 1. With current passing through only Channel V1A's CT, the meter is first calibrated by varying the line voltage attenuation using the resistor network R14 to R23.

Step 2. With current passing through only Channel V1B's CT, the small gain mismatch between the CTs in Channel V1A and V1B is calibrated by shorting the appropriate resistors in the resistor network R8 to R13.

**DESIGN EQUATIONS**

The AD7751 produces an output frequency proportional to the time average value of the product of two voltage signals. The input voltage signals are applied at V1 and V2. The detailed functionality of the AD7751 is explained in the AD7751 data sheet, see *Theory Of Operation*. The AD7751 data sheet also provides an equation that relates the output frequency on F1 and F2 (counter drive) to the product of the rms signal levels at V1 and V2. This equation is shown here again for convenience and will be used to determine the correct signal scaling at V2 in order to calibrate the meter to a fixed constant.

$$Frequency = \frac{5.74 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^2} \quad (1)$$

The meter shown in Figure 1 is designed to operate at a line voltage of 240 V and a maximum current ($I_{MAX}$) of 40 A. However, by correctly scaling the signals on Channel 1 and Channel 2, a meter operating from any line voltage and maximum current could be designed.

The four frequency options available on the AD7751 will allow similar meters (i.e., direct counter drive) with an $I_{MAX}$ of up to 120 A to be designed. The basic current for this meter is selected as 10 A and the current range for accuracy will be 1% Ib to $I_{MAX}$ or a dynamic range of 400 (100 mA to 40 A). The electromechanical register (kWh) will have a constant of 100 imp/kWh, i.e., 100 impulses from the AD7751 will be required in order to register 1 kWhr. IEC1036 Section 4.2.11 specifies that electromagnetic registers have their lowest values numbered in ten division, each division being subdivided into ten parts.

Hence a display with five-plus-one digits is used, i.e., 10,000s, 1,000s, 100s, 10s, 1s, 1/10s. The meter constant (for calibration and test) is selected as 3200 imp/kWh. The on-chip reference circuit of the AD7751 typically has a temperature coefficient of 30 ppm/°C. However, on A grade parts this specification is not guaranteed and may be as high as 80 ppm /°C. At 80 ppm /°C the AD7751 error at –20°C/+60°C would be approximately 0.65%, assuming a calibration at 25°C.

**Current Transformer (CT) Selection**

The CTs and their burden resistors should be selected to maximize the use of the dynamic range on Channel V1A and V1B (current channel). However there are some important considerations when selecting the CTs and the burden resistors for energy metering application. Firstly, one need to select CTs that have good linearity in both their gain and phase characteristics over the range of current specified in the accuracy requirement. For IEC1036, the range is between 5% Ib to $I_{MAX}$. CT manufacturers often recommend the burden resistance to be as small as possible to preserve linearity over large current range. A burden resistance of less than 15 Ω is recommended. Secondly, CT introduces a phase shift between primary and secondary current. The phase shift can contribute to a significant error at low-power factor. Note that at power factor of 0.5, a phase shift as small as 0.1° translates to 0.3% error in the energy reading. In this design, the phase of the voltage channel (V2) is shifted to match the phase shift introduced by the CT to eliminate any phase mismatch between the current and voltage channel. This is achieved by moving the corner frequency of the antialiasing filter in the voltage channel input, see *Corrected Phase Matching between Channels* and *Antialias Filters* in this application note.

**Design Calculations**

Design Parameters:

Line Voltage = 240 V (Nominal)
$I_{MAX}$ = 40 A (Ib = 10 A)
Counter = 100 imp/kWh
Meter Constant = 3200 imp/kWh
CT Turn Ratio = 1:1800
Size of Burden Resistor (Channel 1 A) = 8.2 Ω

100 imp/hour = 100/3600 sec. = 0.027777 Hz
Meter Will Be Calibrated at Ib (10 A)
Power Dissipation at Ib = 240 V × 10 A = 2.4 kW
Frequency on F1 (and F2) at Ib = 2.4 × 0.027777 Hz
= 0.06666667 Hz

Voltage across CT at Ib (V1A) = 10 A/1800 × 8.2 Ω = 45.6 mV.

The gain setting is determined by the signal in V1 (current channel). At $I_{MAX}$ = 40 A, the rms voltage at V1 is 40 A/1800 × 8.2 Ω = 182 mV. It translates to a peak voltage of 258 mV. From Table I of the AD7751 data sheet, it can be seen that the gain of two provides the best utilization of the dynamic range (±330 mV). The setting also provides more than 20% headroom in the event of surge in the current.

To select the $F_{1-4}$ frequency for Equation 1 see the AD7751 data sheet, *Selecting a Frequency for an Energy Meter Application*. From Tables V and VI in the AD7751 data sheet, it can be seen that the best choice of frequency for a meter with $I_{MAX}$ = 40 A is 3.4 Hz ($F_2$). This frequency selection is made by the logic inputs S0 and S1, see Table II in the AD7751 data sheet. The CF frequency selection (meter constant) is selected by using the logic input SCF. The two available options are 64 × F1 (6400 imp/kWh) or 32 × F1 (3200 imp/kWh). For this design, 3200 imp/kWh is selected by setting SCF logic low. With a meter constant of 3200 imp/kWh and a maximum current of 40 A, the maximum frequency from CF is 8.53 Hz. Many calibration benches used to verify meter accuracy still use optical techniques. This limits the maximum frequency which can be reliably read to about 10 Hz. The only remaining unknown from Equation 1 is V2 or the signal level on Channel 2 (the voltage channel).

From Equation 1 on the previous page:

$$0.0666667\,Hz = \frac{5.74 \times 45.56\,mV \times V2 \times 2 \times 3.4\,Hz}{2.5^2}$$

Where: *V*2 = 234.3 mV rms.

Therefore, in order to calibrate the meter, the line voltage needs to be attenuated down to 234.3 mV.

**CALIBRATING THE METER: VOLTAGE CHANNEL CALIBRATION**

From the previous section it can be seen that the meter is simply calibrated by attenuating the line voltage down to 234.3 mV. The line voltage attenuation is carried out by a simple resistor divider as shown in Figure 2. The attenuation network should allow a calibration range of at least ±30% to allow for CT/burden resistance tolerances and the on-chip reference tolerance of ±8%, see the AD7751 data sheet. In addition, the topology of the network is such that the phase matching between Channel 1 and Channel 2 is preserved, even when the attenuation is being adjusted, see *Correct Phase Matching between Channels* in this application note.

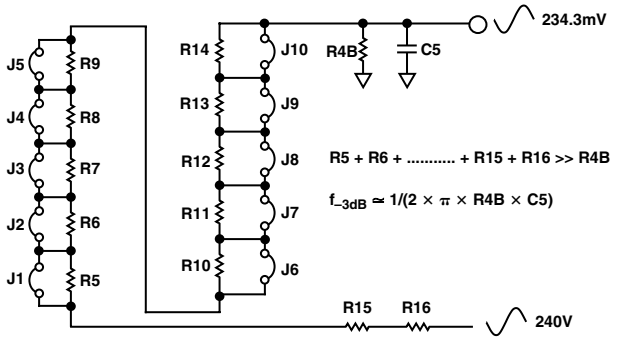



*Figure 2. Attenuation Network for Calibrating the Voltage Channel (V2)*

As can be seen from Figure 2, the –3 dB frequency of this network is determined by R4B and C5. Even with all the jumpers closed, the resistance of R15 (300 kΩ) and R16 (300 kΩ) is still much greater than R4B (887 Ω). Hence varying the resistance of the resistor chain R5 to R14 will have little effect on the –3 dB frequency of the network. The network shown in Figure 2 allows the line voltage to be attenuated and adjusted in the range 170 mV to 399 mV with a resolution of 10 bits or 223 μV. This is achieved by using the binary weighted resister chain R14 to R23. This will allow the meter to be accurately calibrated using a successive approximation technique.

Starting with J1 each jumper is closed in order of ascendance, e.g., J1, J2, J3, etc. If the calibration frequency on CF, i.e., 32 × 100 imp/KWh (at Ib = 10 A, CF is expected to be 2.133 Hz) is exceeded when any jumper is closed, it should be opened again. All jumpers are tested, J10 being the last jumper. Note that jumper connections are made with soldering together the jumper pins across the resistors in the network. This approach is preferred over the use of trim pots, as the stability of the latter over time and environmental conditions is questionable.

Since the AD7751 transfer function is extremely linear, a one-point calibration (at Ib) at unity power factor is all that is needed to calibrate the meter. If the correct precautions have been taken at the design stage no calibration will be necessary at low-power factor (e.g., PF = 0.5).

**CALIBRATING THE METER: MATCHING THE TWO CURRENT SENSOR INPUTS**

A calibration network consisting of six parallel resistors is used to compensate gain variation between the two CTs used to monitor the phase and neutral currents. However, such mismatch is often small and needs to be compensated with a more accurate calibration network. In this design, six resistors are used for this purpose. The primary burden resistors for V1B, R6, and R7, combined to a 8.4 Ω burden (9.1 Ω‖110 Ω = 8.4 Ω). This is about 2.5% above the nominal burden used in V1A. The burden is reduced by connecting the jumpers from J16 to J21. This adds more resistors to be in parallel to the burden, thus reducing the total resistance between the two terminals of the CT. The values of R8 to R13 are chosen carefully so that the resulting resistance values spread out evenly across the calibration range. Closing all jumpers, J16 to J21, represents the lower bound for the calibration range. In our design, the lower bound is at approximately 7.99 Ω, or 2.5% lower than the nominal burden of V1A.

Starting from J16, each jumper is closed in order of ascendance, e.g., J16, J17, J18, etc. If the calibration frequency on CF becomes smaller than the expected value (at Ib = 10 A, CF = 2.133 Hz) after a jumper is closed, the jumper should be opened again. All jumpers are tested, J21 being the last jumper.

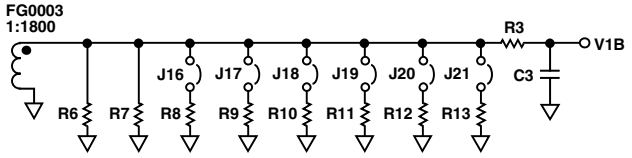



*Figure 3. Calibration Network for V1B*

**CORRECT PHASE-MATCHING BETWEEN CHANNELS**

The AD7751 is internally phase-matched over the frequency range 40 Hz to 1 kHz. Correct phase-matching is important in an energy metering application because any phase mismatch between channels will translate into significant errors at low-power factor. This is easily illustrated with the following example. Figure 4 shows the voltage and current waveforms for an inductive load. In the example shown the current lags the voltage by 60° (PF = 0.5). Assuming pure sinusoidal conditions the power is easily calculated as V rms × I rms × cos (60°).

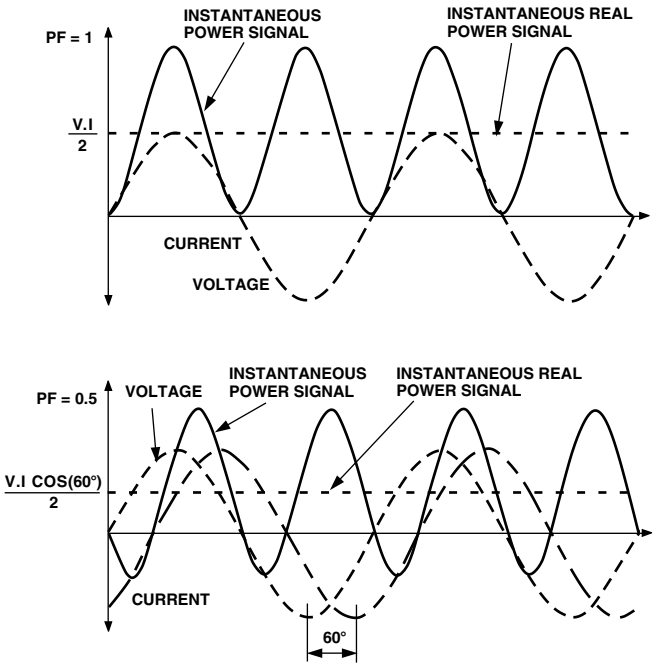



*Figure 4. Voltage and Current (Inductive Load)*

If, however, a phase error ($\phi_e$) is introduced externally to the AD7751, e.g., in the antialias filters, the error is calculated as:

$$[\cos(\delta^\circ) - \cos(\delta^\circ + \phi_e)]/\cos(\delta^\circ) \times 100\% \quad (2)$$

See *Note 3 in Table I.* Where δ is the phase angle between voltage and current and $\phi_e$ is the external phase error. With a phase error of 0.2°, for example, the error at PF = 0.5 (60°) is calculated as 0.6%. As this example demonstrates, even a very small phase error will produce a large measurement error at low-power factor.

The current sensor has an intrinsic phase shift of 0.1°. If it is not compensated, it can introduce a significant error at low-power factor. In this design, the phase is compensated by introducing a 0.1° phase shift in the voltage channel to ensure both the current and voltage inputs are phase matched. This is easily achieved by reducing the resistance in the antialiasing filter in the voltage channel.

**Antialias Filters**

As mentioned in the previous section, one possible source of external phase errors are the antialias filters on Channel 1 and Channel 2. The antialias filters are low-pass filters that are placed before the analog inputs of any ADC. They are required in order to prevent a possible distortion due to sampling called aliasing. Figure 5 illustrates the effects of aliasing.

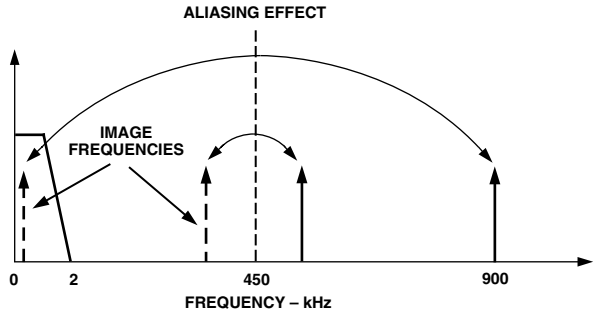



*Figure 5. Aliasing Effects*

Figure 5 shows how aliasing effects could introduce inaccuracies in an AD7751-based meter design. The AD7751 uses two Σ-Δ ADCs to digitize the voltage and current signals. These ADCs have a very high sampling rate, i.e., 900 kHz. Figure 5 shows how frequency components (arrows shown in black) above half the sampling frequency (also known as the Nyquist frequency), i.e., 450 kHz are imaged or folded back down below 450 kHz (arrows shown in grey). This will happen with all ADCs no matter what the architecture is. In the example shown it can be seen that only frequencies near the sampling frequency, i.e., 900 kHz, will move into the band of interest for metering, i.e., 0 kHz–2 kHz. This fact will allow us to use a very simple LPF (Low-Pass Filter) to attenuate these high frequencies (near 900 kHz) and so prevent distortion in the band of interest.

The simplest form of LPF is the simple RC filter. This is a single-pole filter with a roll-off or attenuation of –20 dB/dec.

**CHOOSING THE FILTER –3 dB FREQUENCY**

As well as having a magnitude response, all filters also have a phase response. The magnitude and phase response of a simple RC filter (R = 1 kΩ, C = 33 nF) are shown in Figures 6 and 7. From Figure 6 it is seen that the attenuation at 900 kHz for this simple LPF is greater than 40 dBs. This is enough attenuation to ensure no ill effects due to aliasing.

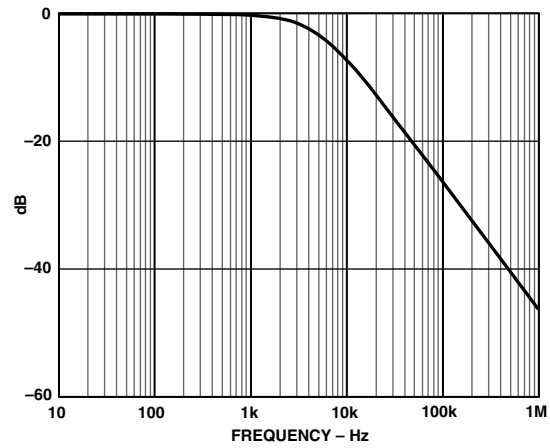



*Figure 6. RC Filter Magnitude Response*

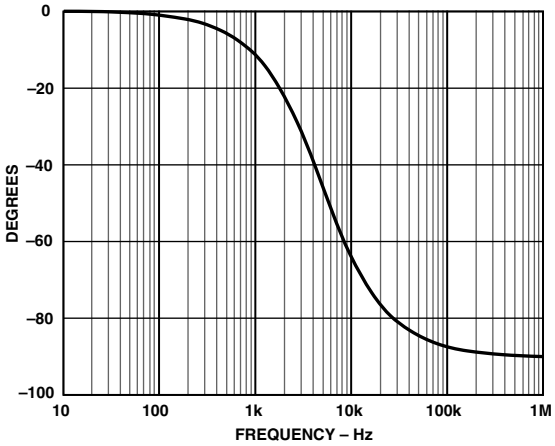



*Figure 7. RC Filter Phase Response*

As explained in the last section, the phase response can introduce significant errors if the phase response of the LPFs on both Channel 1 and Channel 2 are not matched. Phase mismatch can easily occur due to poor component tolerances in the LPF. The lower the –3 dB frequency in the LPF (antialias filter) the more pronounced these errors will be at the fundamental frequency component or the line frequency. Even with the corner frequency set at 4.8 kHz (R = 1 kΩ, C = 33 nF) the phase errors due to poor component tolerances can be significant. Figure 8 illustrates the point. In Figure 8, the phase response for the simple LPF is shown at 50 Hz for R = 1 kΩ ± 10%, C = 33 nF ± 10%. Remember a phase shift of 0.1°–0.2° can cause measurement errors of 0.6% at low-power factor. This design uses resistors of 1% tolerance and capacitors of 10% tolerance for the antialias filters to reduce the possible problems due to phase mismatch. Alternatively the corner frequency of the antialias filter could be pushed out to 10 kHz–15 Hz. However, the corner frequency should not be made too high. This could allow enough high-frequency components to be aliased and cause accuracy problems in a noisy environment.

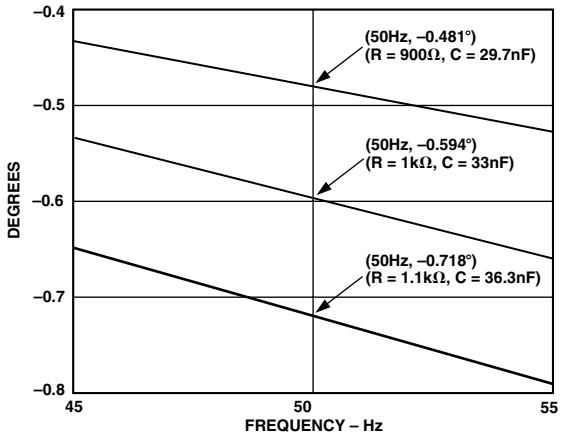



*Figure 8. Phase Shift at 50 Hz Due to Component Tolerances*

Note this is also why precautions were taken with the design of the calibration network on Channel 2 (voltage channel). Calibrating the meter by varying the resistance of the attenuation network will not vary the –3 dB frequency and hence the phase response of the network on Channel 2, see *Calibrating the Meter: Voltage Channel Calibration*. Shown in Figure 9 is a plot of phase lag at 50 Hz when the resistance of the calibration network is varied from 600 kΩ (J1–J10 closed) to 1.2 MΩ (J1–J10 open).

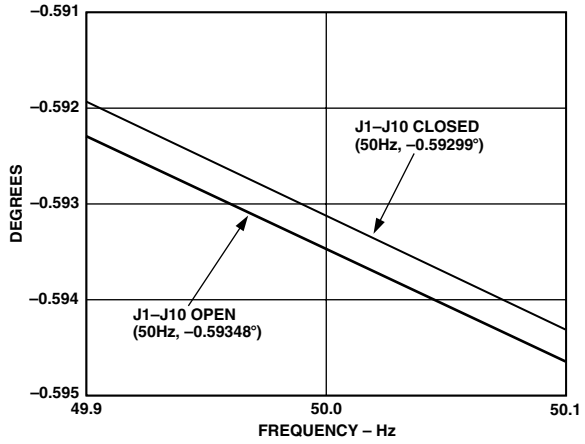



*Figure 9. Phase Shift Due to Calibration*

For the resistor network used for matching the CTs in V1A and V1B, the calibration network is based on altering the burden resistance. High-precision components are used for the RC filters in V1A and V1B. Any mismatch will be caused by the component tolerance. Under normal operation, this mismatch is well within the 12.5% threshold needed to cause AD7751 to indicate a FAULT condition and perform current channel switching.

**NO LOAD THRESHOLD**

The AD7751 has on-chip anticreep functionality. The AD7751 will not produce a pulse on CF, F1, or F2 if the output frequency falls below a certain level. This feature ensures that the energy meter will not register energy when no load is connected. IEC 1036 (1996–09) Section 4.6.4 specifies the start-up current as being not more than 0.4% Ib at PF = 1. For this design the start current is calculated at 7.14 mA or 0.07% Ib, see *No Load Threshold*, AD7751 data sheet.

**POWER SUPPLY DESIGN**

This design uses a simple low-cost power supply based on a capacitor divider network, i.e., C18 and C19. Most of the line voltage is dropped across C18, a 470 nF, 250 V metalized polyester film capacitor. The impedance of C18 dictates the effective VA rating of the supply. However the size of C18 is constrained by the power consumption specification in IEC1036. The total power consumption in the voltage circuit including power supply is specified in Section 4.4.1.1 of IEC1036 (1996–9). The total power consumption in each phase is 2 W and 10 VA under nominal conditions. The nominal VA rating of the supply in this design is 8.5 VA. The total power dissipation is approximately 0.59 W. Figure 10 shows the basic power supply design.

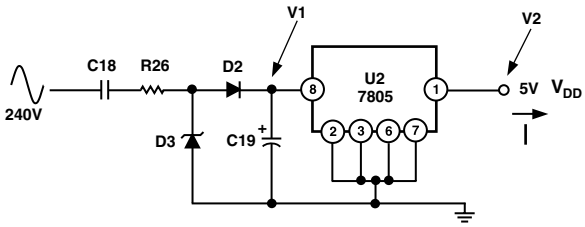



*Figure 10. Power Supply*

The plots shown in Figures 11, 12, 13, and 14 show the PSU performance under heavy load (50 A) with the line voltage varied from 180 V to 250 V. By far the biggest load on the power supply is the current required to drive the stepper motor which has a coil impedance of about 400 Ω. This is clearly seen by looking at V1 (voltage on C19) in the plots below. Figure 11 shows the current drawn from the supply. Refer to Figure 10 when reviewing the simulation plots below.

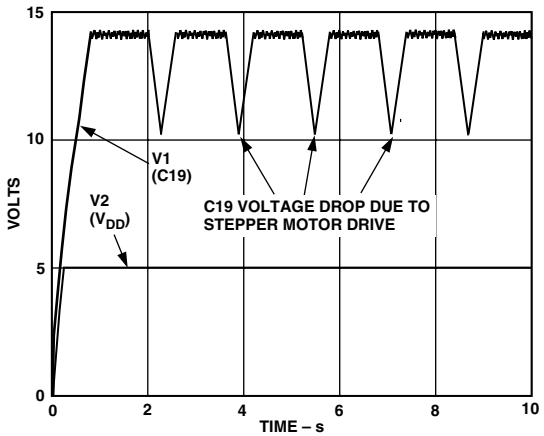



*Figure 11. Power Supply Voltage Output at 220 V and 50 A Load*

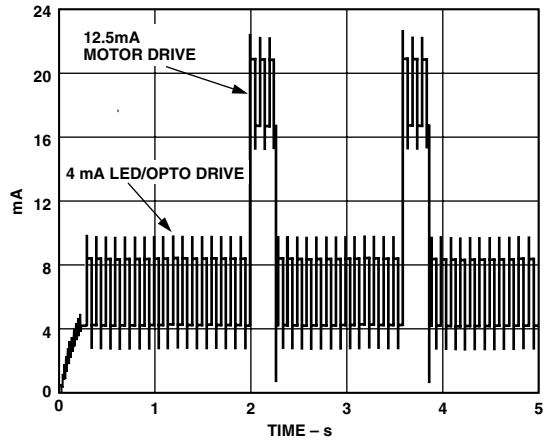



*Figure 12. Power Supply Current Output at 220 V and 50 A Load*

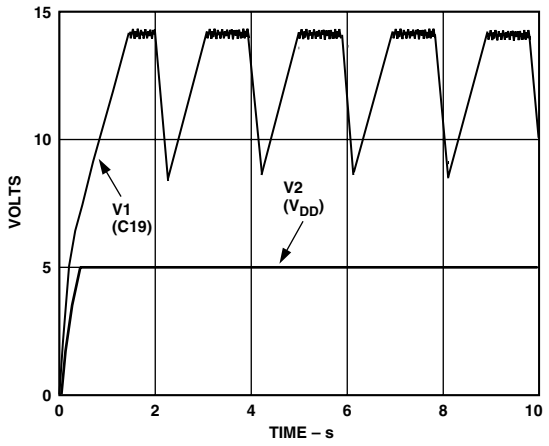



*Figure 13. Power Supply Voltage Output at 180 V and 50 A Load*

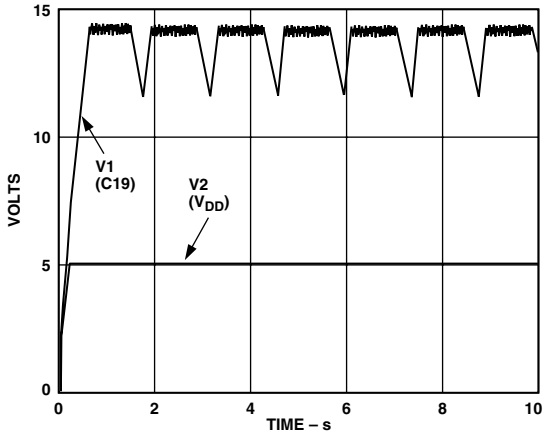



*Figure 14. Power Supply Voltage Output at 250 V and 50 A Load*

**DESIGN FOR IMMUNITY TO ELECTROMAGNETIC DISTURBANCE**

In Section 4.5 of IEC1036 it is stated that "the meter shall be designed in such a way that conducted or radiated electromagnetic disturbances as well as electrostatic discharge do not damage nor substantially influence the meter." The considered disturbances are:

1. Electrostatic Discharge
2. Electromagnetic HF Fields
3. Fast Transience Burst

All of the precautions and design techniques (e.g., ferrite beads, capacitor line filters, physically large SMD resistors, PCB layout including grounding) contribute to a certain extent in protecting the sensitive meter electronics from each form of electromagnetic disturbance. Some precautions (e.g., ferrite beads) however, play a more important role in the presence of certain kinds of disturbances (e.g., RF and fast transience burst). The following discusses each of the disturbances listed above and details what protection has been put in place.

**ELECTROSTATIC DISCHARGE (ESD)**

Although many sensitive electronic components contain a certain amount of ESD protection on-chip, it is not possible to protect against the kind of severe discharge described below. Another problem is that the effects of an ESD discharge is cumulative, i.e., a device may survive an ESD discharge, but this is no guarantee that it will survive multiple discharges at some stage in the future. The best approach is to eliminate or attenuate the effects of the ESD event before it comes in contact with sensitive electronic devices. This holds true for all conducted electromagnetic disturbances. This test is carried out according to IEC1000-4-2, under the following conditions:

- Contact Discharge;
- Test Severity Level 4;
- Test Voltage 8 kV;
- 10 Discharges.

Very often no additional components are necessary to protect devices. With a little care those components already required in the circuit can perform a dual role. For example, the meter must be protected from ESD events at those points where it comes in contact with the "outside world," e.g., the connection to the phase wire. For the current input, AD7751 is connected to two CTs through antialias filters. The CTs insulate the AD7751 from outside contact. The only path for ESD comes from the phase wire to the voltage input. Two ferrite beads

are placed in series with the connection to the line. A ferrite choke is particularly effective at slowing the fast rise time of an ESD current pulse. The high-frequency transient energy is absorbed in the ferrite material rather than being diverted or reflected to another part of the system (the properties of ferrite are discussed later). The PSU circuit is also connected directly to the terminals of the meter. Here the discharge will be dissipated by the ferrite, the line filter capacitor (C18), and the rectification diodes D2 and D3. The analog input V2P is also protected by the large impedance of the attenuation network used for calibration. This antialias (RC) filter can also be enough to protect against ESD damage to CMOS devices. However, some care must be taken with the type of components used. For example, the resistors should not be wire-wound as the discharge will simply travel across them. The resistors should also be physically large to stop the discharge arcing across the resistor. In this design 1/8 W SMD 1206 resistors were used in the antialias filters.

Another very common low-cost technique used to arrest ESD events is to use a spark gap on the component side of the PCB, see Figure 15. However, since the meter will likely operate in an open air environment and be subject to many discharges, this is not recommended at sensitive nodes. Multiple discharges could cause carbon build-up across the spark gap which could cause a short or introduce an impedance that will, in time, affect accuracy. A spark gap was introduced in the PSU after the MOV to take care of any very high-amplitude/fast rise time discharges.

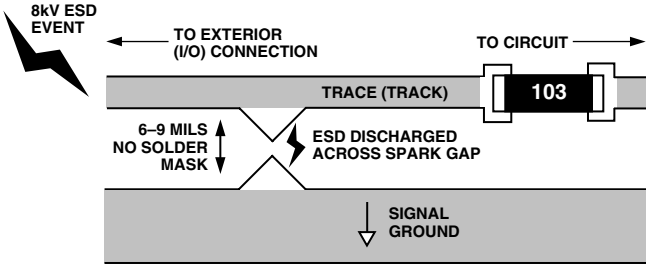



*Figure 15. Spark Gap to Arrest ESD Events*

**ELECTROMAGNETIC HF FIELDS**

Susceptibility of integrated circuits to RF tends to be more pronounced in the 20 MHz–200 MHz region. Frequencies higher than this tend to be shunted away from sensitive devices by parasitic capacitances. In general, at the IC level, the effects of RF in the region 20 MHz–200 MHz will tend to be broadband in nature, i.e., no individual frequency is more troublesome than another. However, there may be higher sensitivity to certain frequencies due to resonances on the PCB. These resonances could cause insertion gain at certain frequencies which, in turn, could cause problems for sensitive devices. By far the greatest RF signal levels are those coupled into the system via cabling. These connection points should be protected. Some techniques for protecting the system are:

1. Minimize Circuit Bandwidth
2. Isolate Sensitive Parts of the System

**Minimize Bandwidth**

In this application the required analog bandwidth is only 2 kHz. This is a significant advantage when trying to reduce the effects of RF. The cable entry points can be low-pass filtered to reduce the amount of RF radiation entering the system. The only direct connection to the cable is at the voltage inputs. The inputs are low-pass filtered to prevent aliasing effects which were described earlier. By Choosing the correct components and adding some additional components (e.g., ferrite beads) these antialias filters can double as effective RF filters. The ferrite bead is an ideal component for this application. The RF radiation is dissipated as heat rather than being reflected or diverted to another part of the system. The ferrite beads Z1 and Z2 perform very well in this respect. Figure 16 shows how the impedance of the ferrite beads varies with frequency.

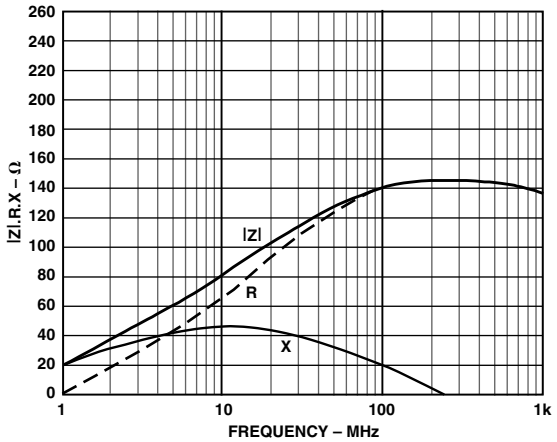



*Figure 16. Frequency Response of the Ferrite Chips (Z1 and Z2)*

From Figure 16 it can be seen that the ferrite material becomes predominately resistive at high frequencies. Also note that the impedance of the ferrite material increases with frequency, causing only high (RF) frequencies to be attenuated.

**ISOLATION**

On the current channels (V1A and V1B), current transformers are used to isolate the line from the system. The system is connected to the phase and neutral lines for the purpose of generating a power supply and voltage channel signal (V2). The ferrite bead (Z1) and line filter capacitor (C18) should significantly reduce any RF radiation on the power supply.

Another possible path for RF is the signal ground for the system. A moating technique has been used to help isolate the signal ground surrounding the AD7751 from the external ground reference point (K6). Figure 18 illustrates the principle of this technique called partitioning or "moating."

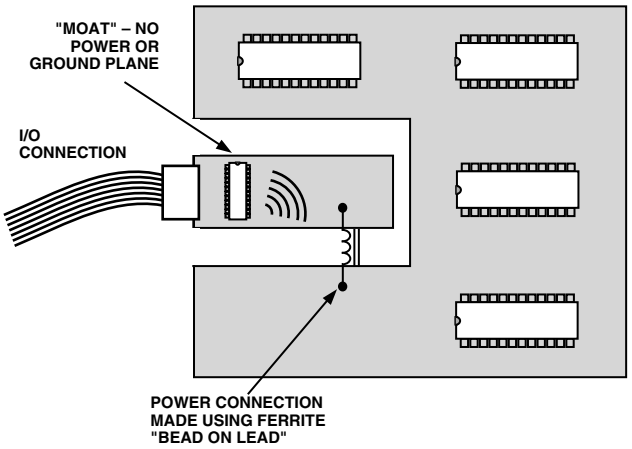



*Figure 17. High-Frequency Isolation of I/O Connections Using a "Moat"*

Sensitive regions of the system are protected from RF radiation entering the system at I/O connection. An area surrounding the I/O connection does not have any ground or power planes. This limits the conduction paths for RF radiation and is called a "moat." Obviously power, ground, and signal connections must cross this moat and Figure 17 shows how this can be safely achieved by using a ferrite bead. Remember that ferrite offers a large impedance to high frequencies—see Figure 16.

**ELECTRICAL FAST TRANSIENCE BURST TESTING (EFT)**

This testing determines the immunity of a system to conducted transients. Testing is carried out in accordance with IEC1000-4-4 under well-defined conditions. The EFT pulse can be particularly difficult to guard against because the disturbance is conducted into the system via external connections, e.g., power lines. Figure 18 shows the physical properties of the EFT pulse used in IEC1000-4-4. Perhaps the most debilitating attribute of the pulse is not its amplitude (which can be as high as 4 kV), but the high-frequency content due to the fast rise times involved. Fast rise times mean high-frequency content which allows the pulse to couple to other parts of the system through stray capacitance, etc. Large differential signals can be generated by the inductance of PCB traces and signal ground. These large differential signals could interrupt the operation of sensitive electronic components. Digital systems are generally most at risk because of data corruption. Analog electronic systems tend to be affected only for the duration of the disturbance.

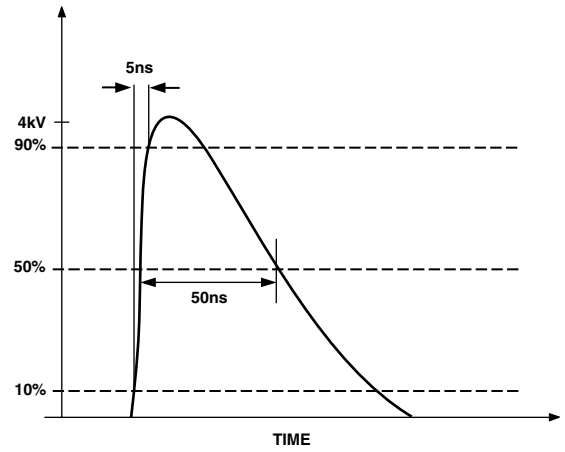



*Figure 18. Single EFT Pulse Characteristics*

Another possible issue with conducted EFT is that the effects of the radiation will, like ESD, generally be cumulative for electronic components. The energy in an EFT pulse can be as high as 4 mJ and deliver 40 A into a 50 Ω load, see Figure 21. Therefore continuous exposure to EFT due to inductive load switching etc., may have implications for the long term reliability of components. The best approach is to protect those parts of the system which could be sensitive to EFT.

The protection techniques described in the last section (Electromagnetic HF Fields) also apply equally well in the case of EFT. The electronics should be isolated as much as possible from the source of the disturbance through PCB layout (i.e., moating) and filtering signal and power connections. In addition, a 10 nF capacitor (C17) placed across the mains provides a low-impedance shunt for differential EFT pulses. Stray inductance due to leads and PCB traces will mean that the MOV will not be very effective in attenuating the differential EFT pulse. The MOV is very effective in attenuating high energy, relatively long duration disturbances, e.g., due to lightening strikes, etc. The MOV is discussed in the next section.

**MOV Type S20K275**

The MOV used in this design was of type S20K275 from Siemens. An MOV is basically a voltage-dependant resistor whose resistance decreases with increasing voltage. The MOV is typically connected in parallel with the device or circuit being protected. During an overvoltage event it forms a low-resistance shunt and thus prevents any further rise in the voltage across the circuit being protected. The overvoltage is essentially dropped across the source impedance of the overvoltage source, e.g., the mains network source impedance. Figure 19 illustrates the principle of operation.

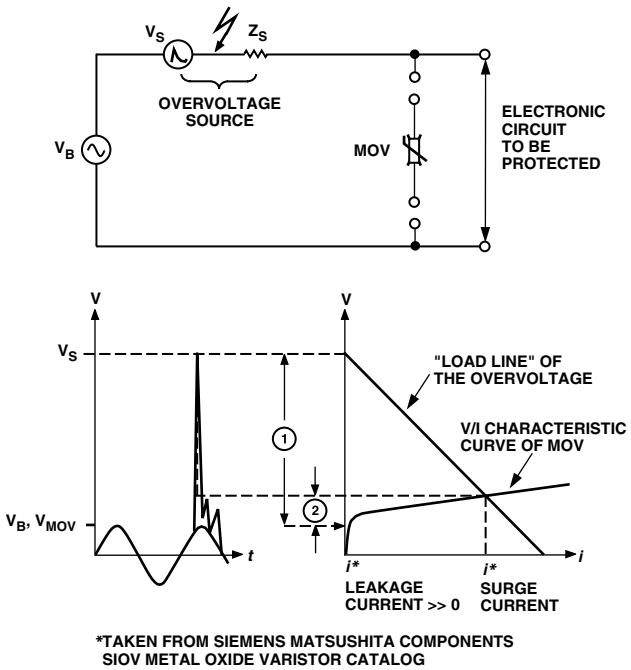



*Figure 19. Principle of MOV Overvoltage Protection*

The plot in Figure 19 shows how the MOV voltage and current can be estimated for a given overvoltage and source impedance. A load line (open-circuit voltage, short-circuit current) is plotted on the same graph as the MOV characteristic curve. Where the curves intersect, the MOV clamping voltage and current can be read. Note, care must be taken when determining the short-circuit current. The frequency content of the overvoltage must be taken into account as the source impedance (e.g., mains) may vary considerably with frequency. A typical impedance of 50 Ω is used for mains source impedance during fast transience (high-frequency) pulse testing. The next section discusses IEC1000-4-4 and IEC1000-4-5 which are transience and overvoltage EMC compliance tests.

**IEC1000-4-4 and the S20K275**

While the graphical technique just described is useful, an even better approached is to use simulation to obtain a better understanding of MOV operation. Siemens Matsushita Components provides SPICE models for all their MOVs and these are very useful in determining device operation under the various IEC EMC compliance tests. For more information on S&M SPICE models and their applications see:

http://www.siemens.de/pr/index.htm

The purpose of IEC1000-4-4 is to determine the effect of repetitive, low-energy, high-voltage, fast rise time pulses on an electronic system. This test is intended to simulate transient disturbances such as those originating from switching transience (e.g., interruption of inductive loads, relay contact bounce, etc.).

Figure 20 shows an equivalent circuit that is intended to replicate the EFT test pulse as specified in IEC1000-4-4. The generator circuit is based on Figure 1 IEC1000-4-4 (1995-01). The characteristics of operation are:

- Maximum Energy of 4 mJ/Pulse at 2 kV into 50 Ω
- Source Impedance of 50 Ω ± 20%
- D.C. Blocking Capacitor of 10 nF
- Pulse Rise Time of 5 ns ± 30%
- Pulse Duration (50% Value) of 50 ns ± 30%
- Pulse Shape as Shown in Figure 18

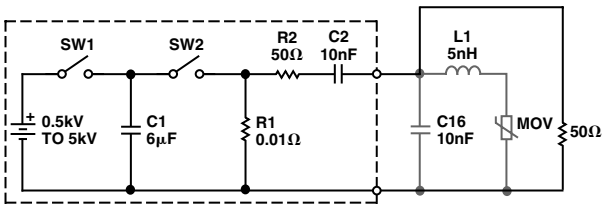



*Figure 20. EFT Generator*

The simulated output of this generator delivered to a purely resistive 50 Ω load is shown in Figure 21. The open-circuit output pulse amplitude from the generator is 4 kV. Therefore the source impedance of the generator is 50 Ω as specified by the IEC1000-4-4, i.e., ratio of peak pulse output unloaded and loaded (50 Ω) is 2:1.

The plot in Figure 21 also shows the current and instantaneous power (V × I) delivered to the load. The total energy is the integral of the power and can be approximated by the rectangle method as shown. It is approximately 4 mJ at 2 kV as per specification.

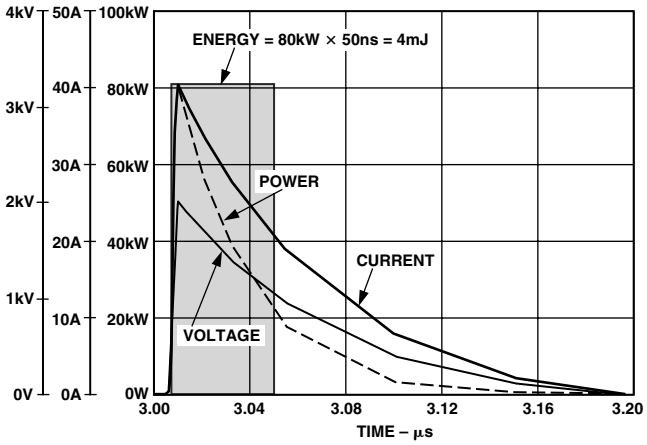



*Figure 21. EFT Generator Output into 50 Ω (No Protection)*

Figure 22 shows the generator output into 50 Ω load with the MOV and some inductance (5 nH). This is included to take into account stray inductance due to PCB traces and leads. Although the simulation result shows that the EFT pulse has been attenuated (600 V) and most of the energy being absorbed by the MOV (only 0.8 mJ is delivered to the 50 Ω load), it should be noted that stray

inductance and capacitance could render the MOV unless. For example, Figure 25 shows the same simulation with the stay inductance increased to 1 μH, which could easily happen if proper care is not taken with the layout. The pulse amplitude reaches 2 kV once again.

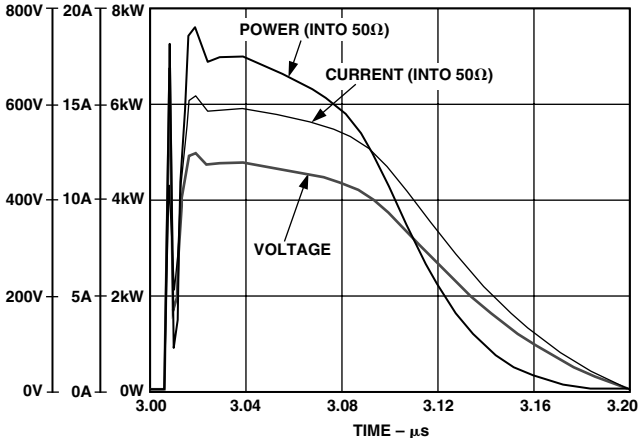



*Figure 22. EFT Generator Output into 50 Ω with MOV in Place*

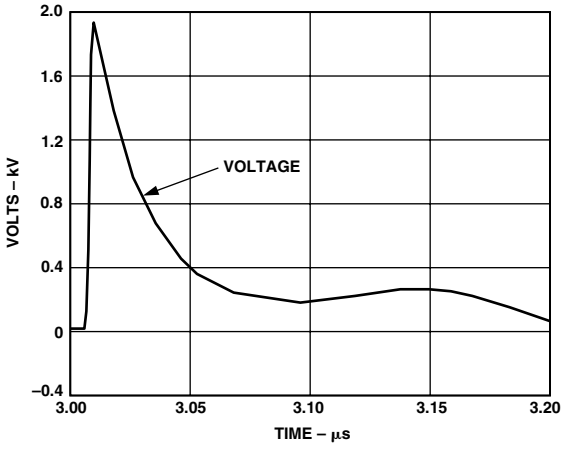



*Figure 23. EFT Generator Output into 50 Ω with MOV in Place and Stray Inductance of 1 μH*

When the 10 nF capacitor (C17) is connected a low-impedance path is provided for differential EFT pulses. Figure 24 shows the effect of connecting C17. Here the stray inductance (L1) is left at 1 μH and the MOV is in place. The plot shows the current through C17 and the voltage across the 50 Ω load. The capacitor C17 provides a low-impedance path for the EFT pulse. Note the peak current through C17 of 80 A. The result is the amplitude of the EFT pulse is greatly attenuated.

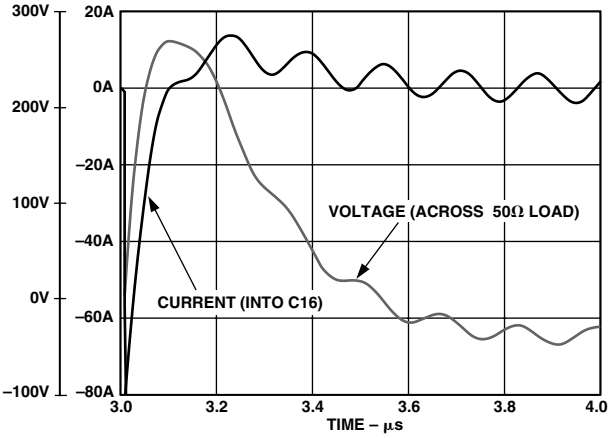



*Figure 24. EFT Generator Output into 50 Ω with MOV in Place, Stray Inductance of 1 μH and C16 (10 nF) in Place*

**IEC1000-4-5**

The purpose of IEC1000-4-5 is to establish a common reference for evaluating the performance of equipment when subjected to high-energy disturbances on the power and interconnect lines. Figure 25 shows a circuit that was used to generate the combinational wave (hybrid) pulse described in IEC1000-4-5. It is based on the circuit shown in Figure 1 of IEC1000-4-5 (1995-02). Such a generator produces a 1.2 μs/50 μs open-circuit voltage, which is why it is referred to as a hybrid generator. The surge generator has an effective output impedance of 2 Ω. This is defined as the ratio of peak open-circuit voltage to peak short-circuit current.

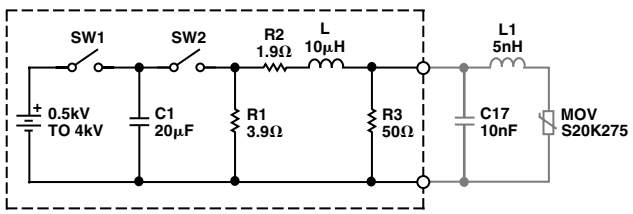



*Figure 25. Surge Generator (IEC1000-4-5)*

Figure 26 shows the generator voltage and current output wave forms. The characteristics of the combination wave generator are:

Open Circuit Voltage
- 0.5 kV to at least 4.0 kV
- Waveform as shown in Figure 26
- Tolerance on open-circuit voltage is ±10%.

Short-Circuit Current
- 0.25 kA to 2.0 kA
- Waveform as shown in Figure 26
- Tolerance on short-circuit current is ±10%

Repetition rate of at least 60 seconds

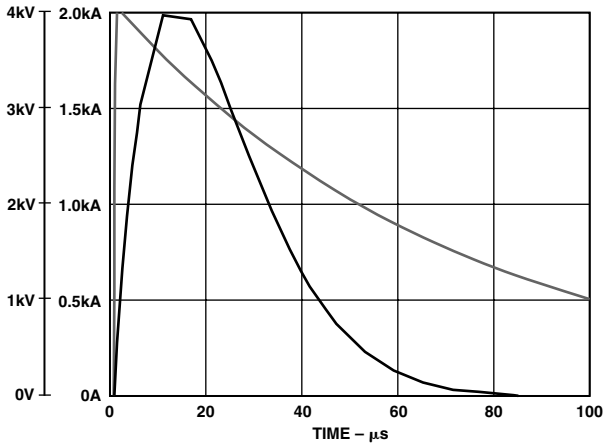



*Figure 26. Open-Circuit Voltage/Short-Circuit Current*

The MOV is very effective in suppressing these kinds of high-energy/long-duration surges. Figure 27 shows the voltage across the MOV when it is connected to the generator as shown in Figure 25. Also shown are the current and instantaneous power waveform. The energy absorbed by the MOV is readily estimated using the rectangle method as shown.

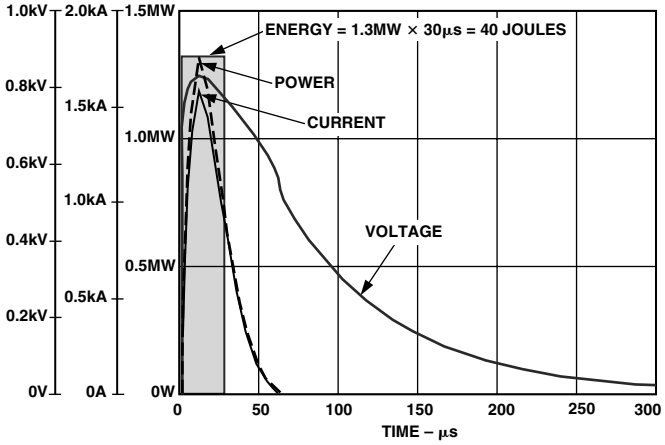



*Figure 27. Energy Absorbed by MOV During 4 kV Surge*

**Derating the MOV Surge Current**

The maximum surge current (and therefore energy absorbed) that an MOV can handle is dependent on the number of times the MOV will be exposed to surges over its lifetime. The life of an MOV is shortened every time it is exposed to a surge event. The data sheet for an MOV device will list the maximum nonrepetitive surge current for an 8 μs/20 μs current pulse. If the current pulse is of longer duration, and if it occurs more than once during the life of the device, this maximum current must be derated. Figure 28 shows the derating curve for the S20K275. Assuming exposures of duration 30 μs and a peak current as shown in Figure 27, the maximum number of surges the MOV can handle before it goes out of specification is about 10. After repeated loading (10 times in the case just described) the MOV voltage will change. After initially increasing, it will decay rapidly.

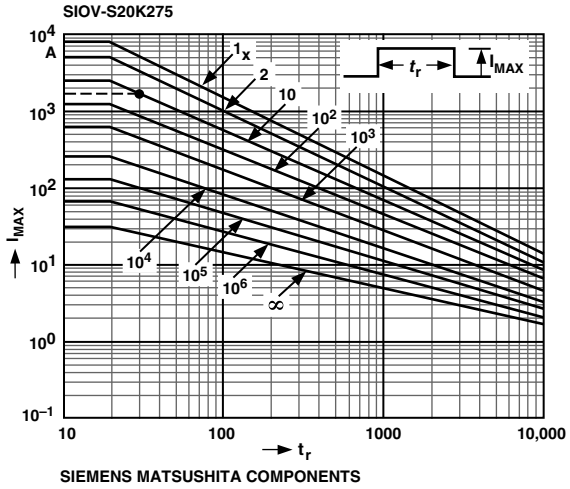



*Figure 28. Derating Curve for S20K275*

**PCB DESIGN**

Both susceptibility to conducted or radiated electromagnetic disturbances and analog performance were considered at the PCB design stage. Fortunately, many of the design techniques used to enhance analog and mixed-signal performance also lend themselves well to improving the EMI robustness of the design. The key idea is to isolate that part of the circuit which is sensitive to noise and electromagnetic disturbances. Since the AD7751 carries out all the data conversion and signal processing, the robustness of the meter will be determined to a large extent by how protected the AD7751 is. In order to ensure accuracy over a wide dynamic range, the data acquisition portion of the PCB should be kept as quiet as possible, i.e., minimal electrical noise. Noise will cause inaccuracies in the analog-to-digital conversion process which takes place in the AD7751. One common source of noise in any mixed-signal system is the ground return for the power supply. Here high-frequency noise (from fast edge rise times) can be coupled into the analog portion of the PCB by the common impedance of the ground return path. Figure 29 illustrates the mechanism.

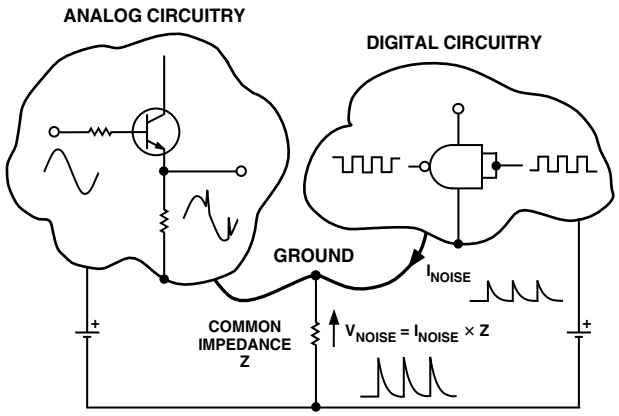



*Figure 29. Noise Coupling via Ground Return Impedance*

One common technique which is used to overcome these kinds of problems is to use separate analog and digital return paths for the supply. Also every effort should be made to keep the impedance of these return paths as low as possible. In the PCB design for the AD7751, separate ground planes were used to isolate the noisy ground returns. The use of ground plane also ensures the impedance of the ground return path is kept as very low. The AD7751 and sensitive signal paths are located in a "quiet" part of the board which is isolated from the noisy elements of the design like the power supply, flashing LED etc. Since the PSU is capacitor- based a substantial current (approximately 35 mA at 240 V) will flow in the ground return back to the wire (system ground). This is shown in Figure 29. By locating the PSU in the digital portion of the PCB this return current is kept away from the AD7751 and analog input signals. This current is at the same frequency as the signals being measured and could cause accuracy issues (e.g., crosstalk between the PSU as analog inputs) if care is not taken with the routing of the return current. Also part of the attenuation network for the Channel 2 (voltage channel) is in the digital portion of the PCB. This helps to eliminate possible crosstalk to Channel 1 by ensuring analog signal amplitudes are kept as low as possible in the analog ("quiet") portion of the PCB. Figure 30 shows the PCB design which was eventually adopted for the watt-hour meter.

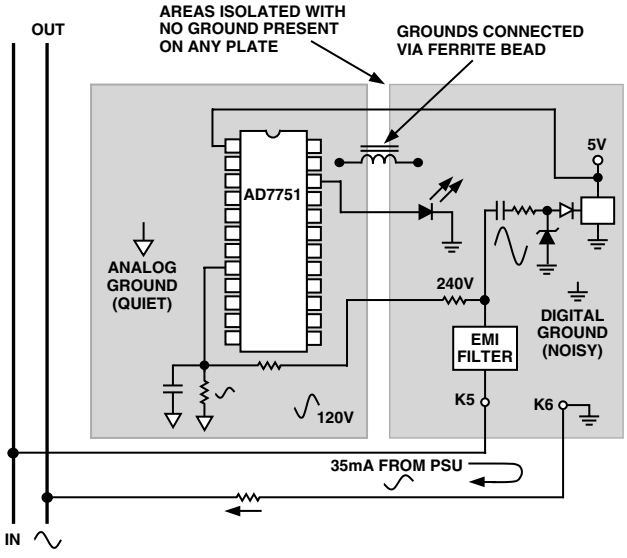



*Figure 30. AD7751 Watt-Hour Meter PCB Design*

The partitioning of the power planes in the PCB design shown in Figure 30 also allows us to implement the idea of a "moat" for the purposes of immunity to electromagnetic disturbances. The digital portion of the PCB is the only place where both phase and neutral wires are connected. This portion of the PCB contains the transience suppression circuitry (MOV, ferrite, etc.) and power supply circuitry. The ground planes are connected via a ferrite bead which help to isolate the analog ground from high-frequency disturbances, see *Design For Immunity to Electromagnetic Disturbances*.

## Meter Accuracy/Test Results

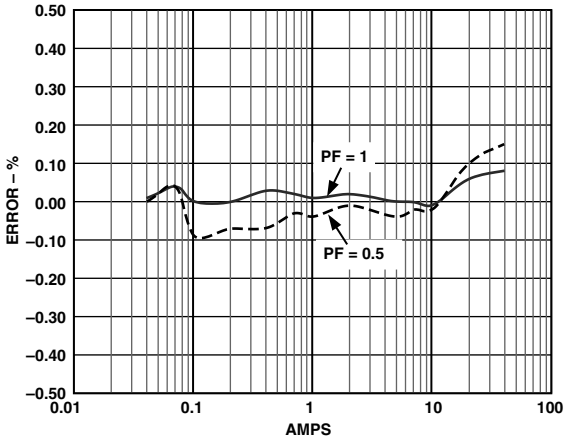



*Figure 31. Measurement Error (% Reading) at 25°C 240 V, PF = 1/+0.5, Freq = 50 Hz*

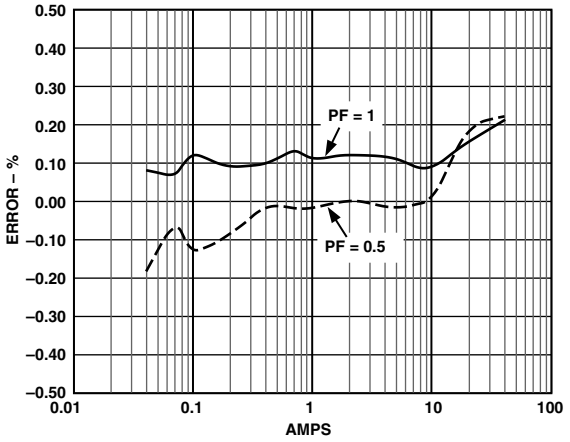



*Figure 32. Measurement Error (% Reading) at 85°C 240 V, PF = 1/+0.5, Freq = 50 Hz*

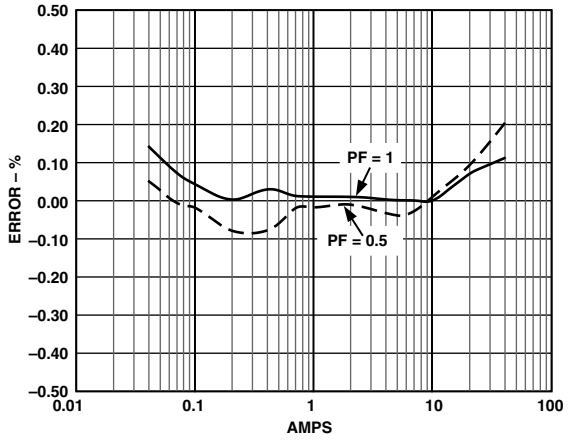



*Figure 33. Measurement Error (% Reading) at –40°C 240 V, PF = 1/+0.5, Freq = 50 Hz*

**ANSI C12.16 and IEC1036**

The ANSI standard governing Solid-State Electricity Meters is ANSI C12.16-1991. Since this application note refers to the IEC 1036 specifications when explaining the design, this section will explain some of those key IEC1036 specifications in terms of their ANSI equivalents. This should help eliminate any confusion caused by the different application of some terminology contained in both standards.

**Class—IEC1036**

The class designation of an electricity meter under IEC1036 refers to its accuracy. For example, a Class 1 meter will have a deviation from reference performance of no more than 1%. A Class 0.5 meter will have a maximum deviation of 0.5% and so on. Under ANSI C12.16 Class refers to the maximum current the meter can handle for rated accuracy. The given classes are: 10, 20, 100, 200 and 320. These correspond to a maximum meter current of 10 A, 20 A, 100 A, 200 A, and 320 A, respectively.

**Ibasic (Ib)—IEC1036**

The basic current (Ib) is a value of current with which the operating range of the meter is defined. IEC1036 defines the accuracy class of a meter over a specific dynamic range, e.g., 0.05 Ib $\leq$ I $\leq$ $I_{MAX}$. It is also used as the test load when specifying the maximum permissible effect of influencing factors, e.g., voltage variation and frequency variation. The closest equivalent in ANSI C12.16 is the Test Current. The Test Current for each meter class (maximum current) is given below:

Class 10 : 2.5 A
Class 20 : 2.5 A
Class 100 : 15 A
Class 200 : 30 A
Class 320 : 50 A

**$I_{MAX}$–IEC1036**

$I_{MAX}$ is the maximum current for which the meter meets rated accuracy. This would correspond to the meter class under ANSI C12.16. For example a meter with an $I_{MAX}$ of 20 A under IEC 1026 would be designated Class 20 under ANSI C12.16.

## BOM

| Part(s) | Details | Comments |
|---|---|---|
| R1, R2, R3 | 1 kΩ, 1%, 1/8 W | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8ENF1001 Digi-Key No. P 1.00K FCT-ND |
| R4A, R4B | 887 Ω, 1%, 1/8 W | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8ENF8870 Digi-Key No. P 887 FCT-ND |
| R5 | 8.2 Ω, 1%, 1/8 W | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8RQF8R2 Digi-Key No. P 8.2 RCT-ND |
| R6 | 9.1 Ω, 1%, 1/8 W | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8ENF9R1 Digi-Key No. P 9.1 RCT-ND |
| R7 | 110 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ111 Digi-Key No. P 110 ECT-ND |
| R8 | 330 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ331 Digi-Key No. P 330 ECT-ND |
| R9 | 620 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ621 Digi-Key No. P 620 ECT-ND |
| R10 | 1.2 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ122 Digi-Key No. P 1.2K JCT-ND |
| R11 | 2.4 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ242 Digi-Key No. P 2.4K JCT-ND |
| R12 | 4.7 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ472 Digi-Key No. P 4.7K JCT-ND |
| R13, R19 | 9.1 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ912 Digi-Key No. P 9.1K JCT-ND |
| R14 | 300 kΩ, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ304 Digi-Key No. P 300K ECT-ND |
| R15 | 150 kΩ, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ154 Digi-Key No. P 150K ECT-ND |
| R16 | 75 kΩ, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ753 Digi-Key No. P 75K ECT-ND |
| R17 | 39 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ393 Digi-Key No. P 39K JCT-ND |
| R18 | 18 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ183 Digi-Key No. P 18K JCT-ND |
| R20 | 5.1 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ512 Digi-Key No. P 5.1K JCT-ND |
| R21 | 2.2 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ222 Digi-Key No. P 2.2K JCT-ND |
| R22 | 1.2 kΩ, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ122 Digi-Key No. P 1.2K JCT-ND |
| R23 | 560 Ω, 5%, 1/16 W, 50 V | SMD 0402 Resistor Surface-Mount, Panasonic, ERJ-2GEJ561 Digi-Key No. P 560 JCT-ND |
| R24, R25 | 300 kΩ, 5%, 1/2 W, 200 V | SMD 2010 Resistor Surface-Mount, Panasonic, ERJ-12ZY304 Digi-Key No. P 300K WCT-ND |
| R26 | 470 Ω, 5%, 1 W | Through-Hole, Panasonic, Digi-Key No. P470W-1BK-ND |
| R27, R28 | 10 kΩ, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ103 Digi-Key No. P 10K ECT-ND |
| R29, R30 | 820 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ821 Digi-Key No. P 820 ECT-ND |
| R31, R32 | 20 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ200 Digi-Key No. P 20 ECT-ND |
| R33 | 10 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ100 Digi-Key No. P 10 ECT-ND |
| C1, C2, C3, C4, C5 | 33 nF, Multilayer Ceramic, 10% 50 V, X7R | SMD 0805 Capacitor Surface-Mount, Panasonic, ECJ-2VB1H333K Digi-Key No. PCC 1834 CT-ND |
| C6, C14 | 10 μF, 6.3 V | EIA Size A Capacitor Surface Chip-Cap, Panasonic, ECS-TOJY106R Digi-Key No. PCS 1106CT-ND – 3.2 mm × 1.6 mm |
| C7, C8, C11, C13, C15, C16 | 100 nF, Multilayer Ceramic, 10%, 16 V, X7R | SMD 0805 Capacitor Surface-Mount, Panasonic, ECJ-2VB1E104K Digi-Key No. PCC 1812 CT-ND |

| Part(s) | Details | Comments |
|---|---|---|
| C9, C10 | 22 pF, Multilayer Ceramic, 5%, 50 V, NPO | SMD 0402 Capacitor Surface-Mount, Panasonic, ECU-E1H220JCQ, Digi-Key No. PCC 220CQCT-ND |
| C12 | 6.3 V, 220 μF, Electrolytic | Through-Hole Panasonic, ECA-OJFQ221, Digi-Key P5604 – ND, D = 6.3 mm, H = 11.2 mm, Pitch = 2.5 mm, dia. = 0.5 mm |
| C17 | 10 nF, 250 V, Class X2 | Metallized Polyester Film Through-hole Panasonic, ECQ-U2A103MN Digi-Key No. P4601-ND |
| C18 | 470 nF, 250 V AC | Metallized Polyester Film Through-Hole Panasonic, ECQ-E6474KF Digi-Key No. EF6474-ND |
| C19 | 35 V, 470 μF, Electrolytic | Through-Hole Panasonic, ECA-1VHG471 Digi-Key P5554 – ND |
| U1 | AD7751AAN | Supplied by ADI – 24 Pin DIP, Use Pin Receptacles (P1-P24) |
| U2 | LM78L05 | National Semiconductor, LM78L05ACM, S0-8 Digi-Key LM78L05ACM-ND |
| U3 | PS2501-1 | Opto, NEC, Digi-Key No. PS2501-1NEC-ND |
| D1, D4 | Low-Current LED | HP HLMP-D150 Newark 06F6429 (Farnell 323-123) |
| D2 | Rectifying Diode | 1 W, 400 V, DO-41, 1N4004, Digi-Key 1N4004DICT-ND |
| D3 | Zener Diode | 15 V, 1 W, DO-41, 1N4744A Digi-Key 1N4744ADICT-ND |
| Z1, Z2 | Ferrite Bead Cores | Axial-Leaded (15 mm × 3.8 mm ) 0.6 mm Lead Diameter Panasonic, EXCELSA391, Digi-Key P9818BK-ND |
| Y1 | 3.579545 MHz XTAL | Quartz Crystal, HC-49 (US), ECS No. ECS-35-17-4 Digi-Key No. X079-ND |
| MOV1 | Metal Oxide Varistors | AC 275 V, 140 Joules FARNELL No. 580-284, Siemens, S20K275 |
| J11–J15 | 0 Ω, 5%, 1/8 W, 200 V | SMD 1206 Resistor Surface-Mount, Panasonic, ERJ-8GEYJ000 Digi-Key No. P0.0ECT-ND |
| P1–P24 | Single Low Profile | Sockets for U1, 0.022" to 0.025" pin diameter ADI stock 12-18-33. ADVANCE KSS100-85TG |
| K1–K10 | Pin Receptacles | 0.037" to 0.043" pin diameter, hex press fit, Mil-Max No. 0328-0-15-XX-34-XX-10-0 Digi-Key ED5017-ND |

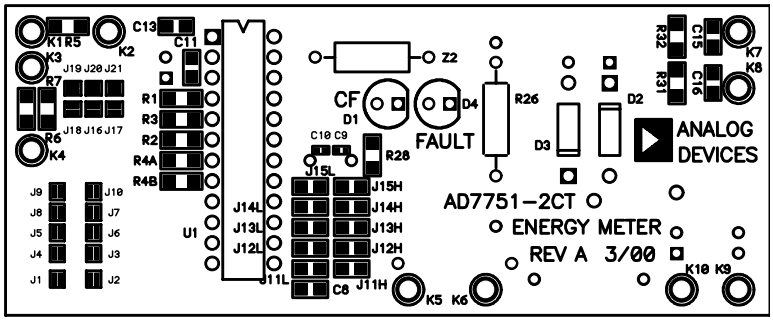



*Figure 34. PCB Assembly (Top Layer)*

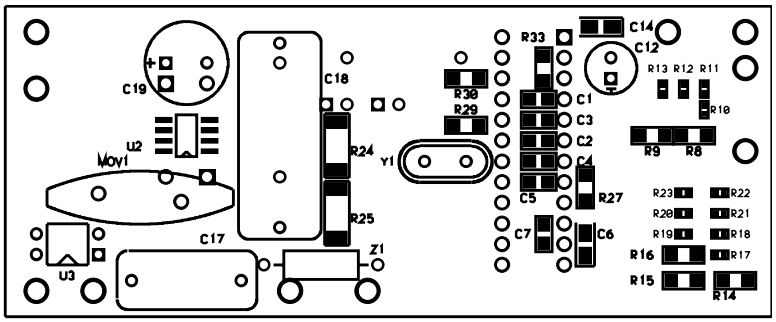



*Figure 35. PCB Assembly (Bottom Layer)*

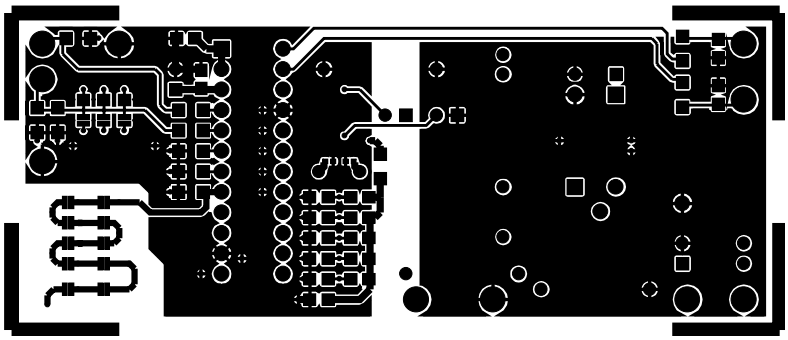


*Figure 36. PCB (Top Layer)*

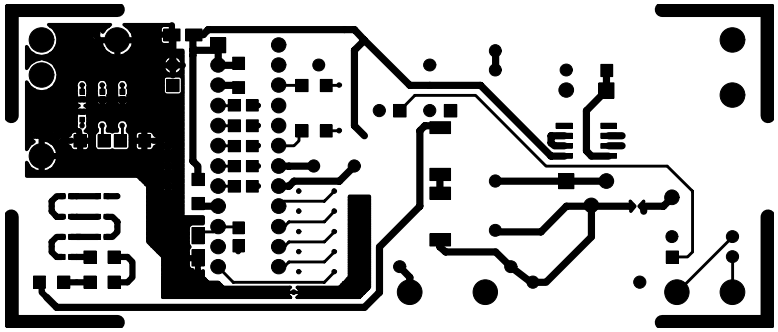
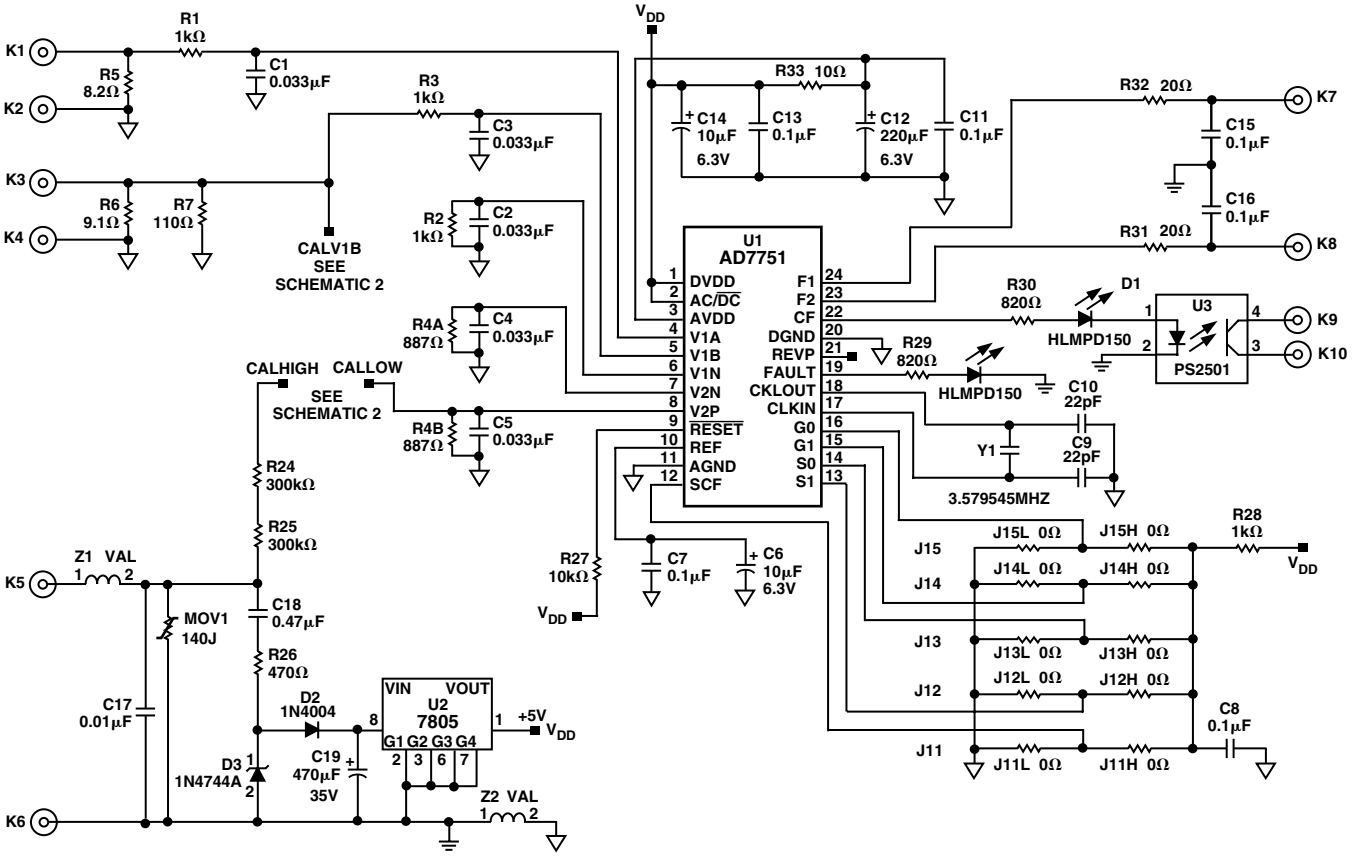
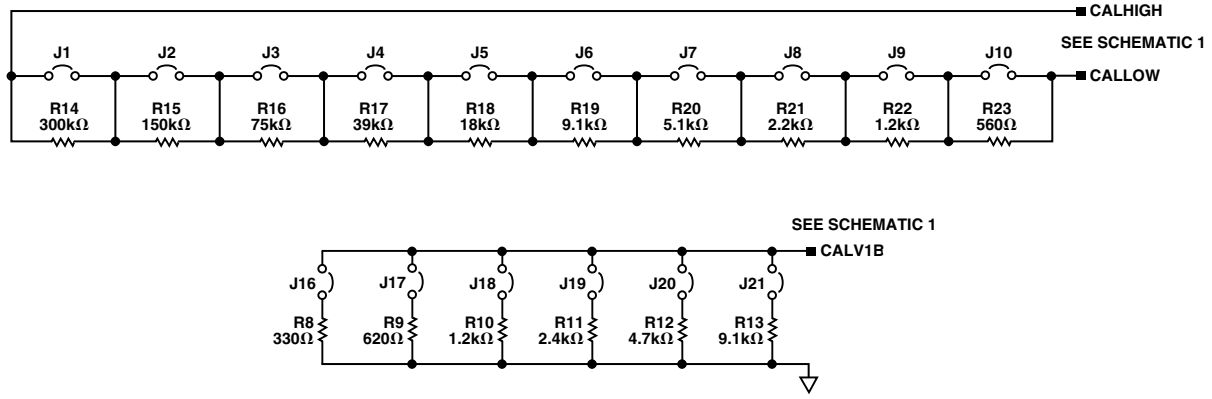


*Figure 37. PCB (Bottom Layer)*




*a. Schematic 1*




*b. Schematic 2*

*Figure 38*